REMARKS

In the Office Action the Examiner rejected Claims 1-21 under U.S.C. Section 103(a) as being unpatentable over Applicant's admitted prior art (AAPA) in view of U.S. Patent Number 6,455,354 to Jiang and U.S. Patent Number 5,733,800 to Moden.

The Examiner contends that with regard to the independent Claims 1, 8 and 15, the AAPA discloses all of the claimed limitations except that the materials for the glob top portion and the underfill portion are not specified. The Examiner further contends that:

> *"It would have been obvious at the time the invention was made to one of ordinary skill in the art to use epoxy as the glob top and acrylic resin as the underfill. The rationale is as follows: Jiang teaches that epoxy is usually used for the glob top, and Moden teaches that such chosen underfill has better thermal, mechanical and viscous properties (Column 9, lines 12-28). One of ordinary skill would have been motivated to use these materials thus make up the device and obtaining better thermal, mechanical and viscous properties. In thus constructed device the glob top material being different than the underfill material." (Office Action, page 2)*

1. <u>The Cited Art References Teach Away From the Suggested Combination</u>

Applicant contends that the Office Action fails to establish a prima facie case of obviousness as there would be not motivation to combine the cited art references as suggested. This is because such references teach away from such combination as the objects or purpose of the inventions of the cited art references would be frustrated by the suggested combination.

The AAPA contemplates that an integrated circuit device that includes a die with solder bumps may be electrically connected to traces disposed upon a polyimide base film.

The Jiang reference pertains to a method of fabricating tape attachment chip-on-board assemblies. The Jiang reference specifically contemplates addressing issues in the fabrication of semiconductor dies that are electrically connected to a semiconductor substrate through wire bonding or TAB (Tape Automated Bonding). (col. 1, lines 28-64) The object of the Jiang invention pertains to two identified problems, namely, bond wire sweep and connection detachment. Bond wire sweep occurs in wire bonded packages, and connection detachment occurs in either TAB connection or bond wires. (col. 2, lines 51-60) The object of the Jiang invention to address these problems would be frustrated if combined with the AAPA as suggested in the Office Action because the AAPA utilizes an integrated circuit device with a solder bump connection (not a TAB connection or bond wires and their associated problems to be specifically solved by the Jiang invention). As such, the cited prior art references themselves teach away from combining the devices of the AAPA and the Jiang reference as these devices utilize competing connection types – solder bump connections, on the one hand, and wire bonding or TAB (Tape Automated Bonding), on the other hand.

A similar teaching away occurs with the suggested combination of the devices of the AAPA and the Moden reference. The Moden reference pertains to an underfill material for a LOC ("leads over chip") type of semiconductor die assemblies (also referred to as an integrated circuit device). One of the shortcomings of the prior art LOC semiconductor die assemblies is that the tape used to bond the lead fingers of the lead frame does not adequately lock the lead fingers in position for the wire bonding process. (col. 1, lines 48-54) The object of the Moden invention to address this problem would be frustrated if combined with the AAPA as suggested in the Office Action because the AAPA utilizes an integrated circuit

device with a solder bump connection (not leads formed form a lead frame and the associated bond wire / tape problems to be specifically solved by the Moden invention). AAPA does not utilize a lead frame or such LOC type of lead, rather the AAPA (not a TAB connection or bond wires and their associated problems to be specifically solved by the Jiang invention). As such, the cited prior art references themselves teach away from combining the devices of the AAPA and the Moden reference as these devices utilize competing connection types – solder bump connections, on the one hand, and wire bonding with tape, on the other hand.

2. Discussion of Prior Art in the Specification

In the Office Action, the Examiner characterizes the AAPA as teaching a "*glob top portion (cover portion) disposed upon the underfill portion and the flex circuit base film for sealing the electrically conductive trace.*" (Office Action, page 2)

Applicant hereby traverses this characterization of the AAPA. The specification in the "Description of Prior Art" section contemplates that an integrated circuit device that includes a die with solder bumps may be electrically connected to traces disposed upon a polyimide base film. Underfill material, which is relatively expensive, is used to attach an integrated circuit device to a base film. In a follow-up touch up process, the same underfill material is used to cover those traces that are exposed between the integrated circuit device and a surrounding opening of a polyimide cover film. (page 2, para. 6 – page 3, para. 7) Thus, there is no discussion of any "glob top" material used in this context of a die with solder bump connections, and cannot be characterized as admitting as much. Therefore the AAPA does not disclose or suggest a glob top material being different than an underfill material.

3. The Jiang Reference

The Jiang reference pertains to a method of fabricating tape attachment chip-on-board assemblies. The Jiang reference specifically contemplates addressing issues in the fabrication of semiconductor dies that are electrically connected to a semiconductor substrate through wire bonding or TAB (Tape Automated Bonding). (col. 1, lines 28-64) As mentioned above, the object of the Jiang invention pertains to two identified problems, namely, bond wire sweep and connection detachment. Bond wire sweep occurs in wire bonded packages, and connection detachment occurs in either TAB connection or bond wires. (col. 2, lines 51-60)

The Jiang reference teaches methods of attaching a semiconductor die 102 to a semiconductor substrate 104. In the embodiment of Figure 3, electrical connections 136 in the form of bond wires used to electrically connect the semiconductor die 102 to a semiconductor substrate 104. In the embodiment of Figure 4, electrical connections 136 in the form of TAB connection are used to electrically connect the semiconductor die 102 to a semiconductor substrate 104. An encapsulant that may be a glob top material is used to encase the electrical connections 136 as respectively shown in Figures 5 and 6. (col. 7, lines 57-67; col. 8, lines 27-49) As the Examiner points out, the glob top material may be made of epoxy or silicone.

However, the Jiang reference does not teach or suggest use of a glob top material in the context of an integrated circuit device that includes a solder bump connection and disposing such integrated circuit device adjacent a flex circuit base film. This is because the glob top material is used to be "globbed" about the bond wires. In contrast, no such bond wires are present in the claimed configuration. Rather, the independent Claims 1, 8 and 15

each recite "an integrated circuit device disposed adjacent the flex circuit base film and including a solder bump connection" and "an electrically conductive trace disposed upon the flex circuit base file, the trace including a contact pad, the contact pad electrically connected to the solder bump connection." Such recited solder bump connection is a fundamentally different application than the wire bonding or tape automated bonding (TAB) that is disclosed by the Jiang reference. Therefore, the Jiang reference fails to teach or suggest the recited "solder bump connection" as required to establish a prima facie case of obviousness.

4. <u>The Moden Reference</u>

The Moden reference pertains to an underfill material for a LOC ("leads over chip") type of integrated circuit device. In this regard, the Moden reference specifically contemplates use of an "underfill material" used in the fabrication of the integrated circuit device itself and not in the context of attaching the integrated circuit device as a finished product to a supporting structure. The underfill material is used to attach a leadframe to a semiconductor die. Subsequently the leadframe is cut to produce leads extending from the semiconductor die to form a semiconductor disk assembly (i.e., the overall integrated circuit device).

For example as shown in Figures 7A and 7B, there is depicted an embodiment of a semiconductor device. A bond lead 112 is attached to a die 102 with an underfill 117. Wires 151 are used to connect the leads 112 to bond pads of an active surface 116 of the die 102. (col, 5, lines 20-22; col. 7, line 60 – col. 8, lines 6) Thus, the "underfill" as contemplated in the Moden reference is in the fabrication of the integrated circuit device itself, between the die and its own leads.

The Moden reference does not contemplate how the finished product is used – i.e., how the finished integrated circuit device is attached to another structure such as a printed circuit board or a base film of a flex circuit as in the case of Applicant's context. Rather, the Moden reference contemplates use of an "underfill" between a "die" and a "bond lead" to form the integrated circuit device itself. As such, the Moden reference does not teach or suggest use of an "underfill portion disposed between the flex circuit base film and the integrated circuit device" as required by independent Claims 1, 8 and 15.

For the foregoing reasons, none of the prior art references relied upon by the Examiner teaches or suggests a "glob top portion" disposed upon an "underfill portion" and a "flex circuit base film" , and so that claim limitation must also be absent from any combination of the references. Applicant therefore submits that all the stated grounds of rejection have been overcome, and therefore all of the pending claims are in condition for allowance. Applicant respectfully requests reconsideration of the rejections of the claims.

Should any additional fees be due please charge Deposit Account No. 19-4330.

Respectfully submitted,

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